Attorney's Docket No.: 10417-076001 / F51-132533M/HW

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLICANT: SHUICHI KIKUCHI, EIJI NISHIBE AND TAKUYA SUZUKI

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EF353806383US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

April 10, 2001
Date of Deposit

Valentin Figueroa
Signature

Valentin Figueroa
Typed or Printed Name of Person Signing Certificate

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1.Fieled of the invention

The present invention relates to a semiconductor device and a method of manufacturing the device, particularly to technique improving operation sustaining voltage characteristic of high sustaining voltage MOS transistor for high voltage of power source (HV-VDD) used for an LCD driver, an EL driver and so on.

2.Description of the related Art

A semiconductor device according to the related art will be described below referring a section view of an LDD type high sustaining voltage MOS transistor shown in Fig. 13.

In Fig. 13, a gate electrode 53 is formed on a P type semiconductor substrate (P-Sub) 51 through a gate insulation film 52. An N+ type source region 54 is formed so as to be adjacent to one end of said gate electrode 53, an N- type drain region 56 is formed facing said source region 54 through a channel region and further separated from the other end of the gate electrode 53, and an N+ type drain region 57 is formed so as to be included in an N- type drain region 56.

In the prior art, a low concentration N- type drain region 56 is formed by thermal diffusion of about 1000℃ to 1100℃ so as to form a gentle slope and a deep diffusion layer.

However, even with such the construction, voltage between source and drain (BVDS: sustaining voltage at OFF) is high, but sustaining voltage (VSUS: sustaining voltage at ON) being operation sustaining voltage of the voltage is about 30 V at most in the prior art.

A mechanism decreasing the above-mentioned operation sustaining voltage will be described below.

In such the N channel type high sustaining voltage MOS transistor, a horizontal bipolar transistor 60 having the drain region 57 as corrector (N+), the source region 54 as emitter (N+), and the semiconductor substrate 51 as base (P) is formed parasitically as shown in Fig. 14 and Fig. 15. Decreasing of operation sustaining voltage VSUS even if voltage between source and drain BVDS being sustaining voltage at OFF is caused by ON of the parasitical bipolar transistor 60. Thus, operation range of the N channel type high sustaining voltage MOS transistor is limited and operation at all over the range is difficult.

An operation of said bipolar transistor 60 will be described below.

AS shown in Fig. 14, gate voltage (VG) (>Vt: threshold voltage) is added to the gate electrode 53, voltage of a drain electrode (VD) (»VG) contacting the drain region 57 is added, and a positive feedback loop described later (refer Fig. 16) is formed in the case of ON of the MOS transistor.

That is, ① avalanche multiplication generates in a depletion layer by electron of a channel region 62 accelerated at a depletion layer near the drain region 57 so as to generate a pair of an electron and a hole. ② Said hole flows in the substrate (substrate current: ISub) ③ Said substrate current (ISub) generates voltage slope in the semiconductor substrate 51 to raise substrate voltage. ④ Junction between the source region 54 and the substrate 51 is biased to forward direction. ⑤ Electron is implanted from the source region 54 to the substrate 51. ⑥ The implanted electron reaches the drain region 57 and further occurs avalanche multiplication.

Thus, by forming the positive feedback of ① to ⑥, large current flows in the device so as to break the device.

Therefore, in design of the N channel type high sustaining voltage MOS transistor, conditions of the design are set considering the above-mentioned phenomenon. First, a transistor construction decreasing substrate current (ISub) is adopted because operation sustaining voltage (VSUS) becomes small as substrate current (ISub) becomes large, and second, the conditions are decided so as to decrease substrate current (ISub) at an actually used region.

Fig. 7 is a substrate current (ISub) vs. gate voltage (VG) characteristic view, in the figure, double humps characteristic of substrate current (ISub) at high region in gate voltage (VG) rises about the conventional N channel type

high sustaining voltage MOS transistor (shown with a dotted line in the figure). Therefore, operation sustaining voltage (VSUS) is low as shown in drain current (ID) vs. drain voltage (VD) characteristic view of Fig. 8 and a characteristic view showing operation sustaining voltage of Fig. 9.

The double humps characteristic is caused by concentration of electric field by spreading the depletion layer near the N+ drain region at high region in gate voltage (VG).

Although it is considered to increase ion implantation volume(doze) and to rise concentration of N- type drain region as shown in Fig. 9 to improve operation sustaining voltage (VSUS), the conventional semiconductor device is not improved enough in sustaining voltage as shown with white circles. Because concentration of end portion A of the N- type drain region 56 shown in Fig. 13 rises conversely, problems of increase of short channel effect by that depletion layer spreads to the channel region 55 direction, increase of snap back phenomenon by increase of peak value of substrate current (ISub), and further decrease of voltage between source and drain (BVDS) occur. Therefore, there is not effective means improving operation sustaining voltage.

Therefore, an object of the invention is to provide a semiconductor device capable of improving operation sustaining voltage and a method of manufacturing the device.

SUMMARY OF THE INVENTION

A semiconductor device of the invention has a gate electrode formed extending on a first and second gate insulation films formed on one conductive type semiconductor substrate, a reverse conductive type source region adjacent to one end of said gate electrode, a first low concentration reverse conductive type drain region formed facing said source region through a channel region, having high impurity concentration peak at a position of the predetermined depth at least in said substrate under said first gate insulation film, and formed so that high impurity concentration becomes low at a region near surface of the substrate, a second concentration reverse conductive type drain region formed so as to range to the first low concentration reverse conductive type drain region, and a third concentration reverse conductive type drain region separated from the other end of said gate electrode and included in said second concentration reverse conductive type drain region.

Thus, it is possible that the first concentration reverse conductive type drain region under the first gate insulation film where the gate electrode is formed lower in high impurity concentration than the second concentration reverse conductive type drain region of an active region and electric field concentration at end portion of the gate electrode through the first gate insulation film is depressed so as to

design high sustaining voltage.

A semiconductor device of the invention has high impurity concentration peak at a position of the predetermined depth in said substrate at a region spanning from one end of said first gate insulation film to said third concentrate reverse conductive type drain region, and the fourth concentration reverse conductive type layer is formed so that high impurity concentration becomes low at a region near surface of the substrate.

A method of manufacturing a semiconductor device has process for ion-implanting a reverse conductive type impurity in the predetermined region of one conductive type semiconductor substrate, process for forming a first gate insulation film field-oxidizing the predetermined region of said substrate, forming a first concentration reverse conductive type drain region under the first gate insulation film diffusing said impurity ion-implanted, and forming a second concentration reverse conductive type drain region so as to range to the first concentration reverse conductive type drain region, process for forming a gate electrode so as to span from the first gate insulation film to the second gate insulation film after forming the second gate insulation film on said substrate except said first gate insulation film, and process for forming a reverse conductive type source region so as to be adjacent to one end of said gate electrode, and

forming a third concentration reverse conductive type drain region facing said source region through a channel region, separated from the other end of said gate electrode, and included in said second concentration reverse conductive type drain region.

A method of manufacturing a semiconductor device has process for forming the fourth concentration reverse conductive type layer so as to span from one end portion of said first gate insulation film to said third concentration reverse conductive type drain region after forming said third concentration reverse conductive type drain region.

A method of manufacturing a semiconductor device has process for forming a fourth concentration reverse conductive type layer having high impurity concentration peak at a position of the predetermined depth in said substrate at a region spanning from a position having the predetermined space from one end portion of said first gate insulation film to said third concentration reverse conductive type drain region, and is formed so that high impurity concentration becomes low at a region near surface of the substrate after forming said third concentration reverse conductive type drain region.

A method of manufacturing a semiconductor device has said forming process of the fourth concentration reverse conductive type layer wherein phosphorus ion is ion-implanted with high acceleration energy of about 100 KeV to 200 KeV.

A method of manufacturing a semiconductor device has said forming process of the fourth concentration reverse conductive type layer wherein ion implantation is carried out at a region spanning from a position separated the predetermined space from said first gate insulation film to said third concentration reverse conductive type drain region by using a photo-resist as a mask.

A method of manufacturing a semiconductor device has said forming process of the fourth concentration reverse conductive type layer wherein ion implantation is carried out at a region spanning from a position separated the predetermined space from the first gate insulation film to said third concentration reverse conductive type drain region by using a side wall insulation film formed at a side wall portion of said first gate insulating film as a mask.

A method of manufacturing a semiconductor device has said forming process of the fourth concentration reverse conductive type layer wherein said fourth concentration reverse conductive type layer is formed at a region spanning from a position separated the predetermined space from the first gate insulation film to said third concentration reverse conductive type drain region by ion implantation from oblique upper side of the first gate insulation film by using said gate insulation film as a mask.

A method of manufacturing a semiconductor device has said

forming process of the fourth concentration reverse conductive type layer wherein said fourth concentration reverse conductive type layer is formed at a region spanning from a position separated the predetermined space from the first gate insulation film to said third concentration reverse conductive type drain region by ion-implanting from oblique upper side of the first gate insulation film by using a photo-resist formed so as to cover said first gate insulation film as a mask.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a first section view showing a method of manufacturing a semiconductor device of a first embodiment of the present invention.

Fig. 2 is a second section view showing a method of manufacturing a semiconductor device of a first embodiment of the present invention.

Fig. 3 is a third section view showing a method of manufacturing a semiconductor device of a first embodiment of the present invention.

Fig. 4 is a fourth section view showing a method of manufacturing a semiconductor device of a first embodiment of the present invention.

Fig. 5 is a view showing substrate concentration distribution of the semiconductor device of the first embodiment of the present invention.

Fig. 6 is a section view showing a method of manufacturing

a semiconductor device of a second embodiment of the present invention.

Fig. 7 is a view showing substrate current (ISub) vs. gate voltage (VG) of a semiconductor device of the invention and the conventional semiconductor device.

Fig. 8 is a view showing drain current (ID) vs. drain voltage (VD) of a semiconductor device of the invention and the conventional semiconductor device.

Fig. 9 is a view showing operation sustaining voltage of a semiconductor device of the invention and the conventional semiconductor device.

Fig. 10 is a section view showing a method of manufacturing a semiconductor device of a third embodiment of the present invention.

Fig. 11 is a section view showing a method of manufacturing a semiconductor device of a fourth embodiment of the present invention.

Fig. 12 is a section view showing a method of manufacturing a semiconductor device of a fifth embodiment of the present invention.

Fig. 13 is a section view showing the conventional semiconductor device.

Fig. 14 is a section view of the semiconductor device for describing the mechanism of the conventional operation sustaining voltage drop.

Fig. 15 is a view showing the equivalent circuit of the conventional parasitic bipolar transistor.

Fig. 16 is a view showing a positive feedback loop for describing the mechanism of the conventional operation sustaining voltage drop.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of a semiconductor device and a method of manufacturing the same of the invention will be described below referring figures.

In a semiconductor device of a first embodiment according to the invention, a first gate insulation film 4 and a second gate insulation film 6 are formed on one conductive type semiconductor substrate, for example, P type semiconductor substrate (P-SuB) 1, and a gate electrode 7 is formed so as to span from the first gate insulation film 4 to the second gate insulation film 6 as Fig. 4. A high concentration reverse conductive (N+) type source region 9 is formed so as to be adjacent to one end of said gate electrode 7, a first low concentration reverse conductive (N--) type drain region 5A is formed so as to face said source region 9 through a channel region under the gate electrode 7, a second low concentration reverse conductive (N-) type drain region 5B is formed so as to range to the first low concentration reverse conductive (N--) type drain region 5A, and further, a high (third) concentration reverse conductive (N+) type drain region 10 is

formed so as to be separated from the other end of said gate electrode 7 and included in said second low concentration N-type drain region 5B.

Thus, a low concentration reverse conductive type drain region 5 is formed so as to be high in high impurity concentration from the end of the gate electrode 7 to said third concentration reverse conductive (N+) type drain region 10. That is, the low concentration reverse conductive type drain region 5 is formed so that high impurity concentration becomes high from the first low concentration reverse conductive (N--) type drain region 5A to the second low concentration reverse conductive (N-) type drain region 5B.

A method of manufacturing the above-mentioned semiconductor device will be described below.

First, an ion implantation layer 3 is formed by ion-implanting N type impurity on a drain forming region on a P type semiconductor substrate 1 by using a photo-resist 2 as a mask as shown in Fig. 1. In the process, as the N type impurity, phosphorus ion ($^{31}P^{+}$) for example is ion-implanted with about 100 KeV in acceleration voltage and 4 x $10^{12}/cm^2$ to 6 x $10^{12}/cm^2$ (6 x $10^{12}/cm^2$ in the embodiment) in implantation ~~volume~~ dose.

Next, by field oxidation of the predetermined region of the substrate 1, a first gate insulation film 4 consisting of a field oxidation film of 800 nm thickness is formed as shown in Fig. 2. In the process, the field oxidation film is formed

by field oxidation of about 1000 ℃, 1 hour in N_a atmosphere and 5 hours in O_a atmosphere.

Next, in the process, phosphorus ion in said ion implantation layer 3 is diffused, the first low concentration reverse conductive (N--) type drain region 5A is formed under said first gate insulation film 4, and the second low concentration reverse conductive (N-) type drain region 5B is formed so as to range to the first low concentration reverse conductive (N--) type drain region 5A.

Here, the semiconductor of the invention is characterized in ion-implanting for forming an N type drain region before forming the field oxidation film and letting between under the field oxidation film (the first gate insulation film 4) and an active region have impurity distribution.

That is, a low concentration N type drain region 5 is formed at a region including under the first gate insulation film 4 formed by well-known LOCOS (Local oxidation of silicon) as shown in Fig. 2. The under part of the first gate insulation film 4 of the drain region 5 is formed low in impurity comparing with other region in the drain region 5. First, by field oxidation after ion-implanting phosphorus ion ($^{31}P^+$) into a forming region of said drain region 5 with 4 x $10^{12}/cm^2$ to 6 x $10^{12}/cm^2$ in implantation ~~volume~~ dose as above-mentioned, phosphorus ion ($^{31}P^+$) is taken in the first gate insulation film 4 at growth region of said first gate insulation film 4 at

oxidation, the low concentration N-- type drain region 5A is formed under the first gate insulation film 4, and the N- type drain region 5B rather higher in impurity than the N-- type drain region 5A is formed so as to range to the N-- type drain region 5A (the other end of the first gate).

As described above, by field oxidation after ion-implanting phosphorus ion ($^{31}P^{+}$) at the forming region of said drain region 5 and ion-implanting the P type impurity for forming the channel stopper layer under the forming region of the first gate insulation film 4, The phosphorus ion ($^{31}P^{+}$) is taken in the first gate insulation film4 at the growth part of said gate insulation film 4 at oxidation. By ion-implanting a reverse conductive P type impurity to phosphorus ion (for example, boron ion ($^{11}B^{+}$), the low concentration N-- type drain region is formed under the first gate insulation film 4. Further, since the process uses ion implantation process of the P type impurity for forming the channel stopper layer, number of manufacturing process is not decreased and operation efficiency is good.

As shown in Fig. 3, by forming a conductive film, for example, a polysilicon film at the entire surface after forming the second gate insulation film 6 of about 100 nm thickness carrying out thermal oxidation at region except the first gate insulation film 4 on said substrate 1 and by patterning the polysilicon film using well-known patterning technique, the

gate electrode 7 of 400 nm in thickness is formed so as to span from said first gate insulation film 4 to the second gate insulation film 6.

As shown in Fig. 4, arsenic ion ($^{75}As^{+}$) for example is ion-implanted on the predetermined region on a source forming region and said low concentration drain region 5 with 80 KeV in acceleration voltage and about 6 x $10^{15}/cm^2$ in implantation dose volume by using a photo-resist 8 having openings as a mask. A high concentration N+ type source region 9 is formed so as to be adjacent to one end of said gate electrode 7, and a high (third) concentration N+ type drain region 10 separated from the other end of the gate electrode 7 and included in said low concentration (n-) type drain region 5B is formed.

In concentration distribution of the semiconductor device formed as above, as shown in Fig. 5, concentration rises gradually from a drain end portion A of a channel side to the N+ type drain region 10. As concentration of the end portion A of the low concentration N type drain region 5 becomes low (concentration of the N- type drain region 5A becomes lower than concentration of the N- type drain region 5B), voltage between source and drain (BVDS) is maintained and operation sustaining voltage (VSUS) is improved.

Thus, by ion-implanting for forming low concentration drain region before field oxidation, the low concentration N type drain region 5 having concentration distribution at under

part of the first gate insulation film 4 and the active region is formed so that operation efficiency is good.

An another embodiment of the invention will be described.

First, the second embodiment is useful in case to raise more operation sustaining voltage (VSUS) in the semiconductor device of the above-mentioned first embodiment. As shown in Fig. 6, by forming an N type layer 11 which is lower in concentration than the N+ type drain region 10 and higher than said N- type drain region 5B (so called middle concentration) so as to surround the N+ type drain region 10, operation sustaining voltage (VSUS) is further improved.

In the method of manufacturing the semiconductor device of the embodiment, by ion-implanting phosphorus ion ($^{31}P^{+}$) into a forming region of said drain region 5 with about 160 KeV in acceleration voltage and about 2 x $10^{12}/cm^2$ in implantation volume as shown in Fig. 6 after the method of manufacturing the semiconductor device of the above-mentioned first embodiment (processes of Fig. 1 to Fig. 4), the N type layer 11 is formed.

By the process, the N+ type drain region 10 is surrounded by the above-mentioned N type layer 11 maintaining concentration of channel side drain region end portion low concentration by the N—type drain region 5A. AS described above, by surrounding said high concentration N+ drain region 10 with the middle concentration N type layer 11 and by letting

depletion layer not extend to the N+ type drain region, the semiconductor device of the invention removes double humps characteristic and can decrease substrate current (ISub) at high gate voltage (VG) region as shown with a solid line in Fig. 7. Thus, operation sustaining voltage (VSUS) improves as shown in Fig. 8 and Fig. 9. Especially, sustaining voltage improves extremely at high gate voltage (VG) and high drain current (ID).

Next, a third embodiment of the invention will be described.

The characteristic of the semiconductor device of the third embodiment is that a middle concentration N type layer 11A is formed having the predetermined space (L) from one end portion (drain side) of the ~~gate electrode 7~~ gate insulation 4 through said first gate insulation film 4 as shown in Fig. 10. Since electric field concentration at the end portion of the gate electrode 7 by forming the N type layer 11A having the predetermined space (L) from one end portion the ~~gate electrode 7~~ gate insulation 4, higher sustaining voltage is designed.

In the above-mentioned method of manufacturing the semiconductor device, in the process of Fig. 6 described at the above-mentioned second embodiment, a middle concentration N type layer 11A is formed near the N+ type drain region 10 included in said N- type drain region having the predetermined space (L) from one end portion of said gate electrode 7 "insulation film 4" as shown

in Fig. 10 by ion-implanting phosphorus ion ($^{31}P^{+}$), for example, with about 160 KeV in acceleration voltage and about 2 x $10^{12}/cm^2$ in implantation volume forming a photo-resist 12 so as to overlap with the predetermined space from the one end portion (drain side) of the gate electrode. Therefore, a space from the gate ~~electrode 7~~ (L) can be set freely by adjusting overlap quantity to the gate electrode 7 through the first gate insulation film 4 at forming the photo-resist 12.

An another embodiment forming the above-mentioned middle concentration N type layer having the predetermined space from one end (drain side) of the gate electrode 7 through the above-mentioned first gate insulation film 4 will be described.

First, in a fourth embodiment, the above-mentioned construction is realized by forming a side wall insulation film 13 so as to cover a side wall portion of the first gate insulation film 4 ion-implanting for forming N type layer by using a side wall insulation film 13 as a mask as shown in Fig. 11.

That is, after process of Fig. 4 described in the first embodiment, an insulation film is formed by CVD method. After that, the side wall insulation film 13 is formed at a gate electrode 7 and a side wall portion of the first gate insulation film 4 by isotropic etching the insulation film.

Then, a middle concentration N type layer 11B is formed near the N+ type drain region 10 included in said N- type drain region 5B having the predetermined space (L) from the other

end portion of said gate ~~electrode 7~~ insulation 4 by ion-implanting phosphorus ion ($^{31}P^{+}$), for example, with about 160 KeV in acceleration voltage and about 2 x $10^{12}/cm^2$ in implantation ~~volume~~ dose by using said first gate insulation film 4 and the side wall insulation film 13 as a mask.

Thus, in the fourth embodiment, since the side wall insulation film 13 formed at the side wall portion of the first gate insulation film 4 instead of the photo-resist 12 such as the second embodiment is used for a part of a mask, positioning margin of forming the N type layer to the gap of mask matching worried at using the photo-resist 12 can be ensured. That is, in the embodiment, a space (L) from the end portion of the gate electrode 7 to the position forming the N type layer 11B can be adjusted freely by thickness of the insulation film for forming the side wall insulation film.

Further, a fifth embodiment will be described.

Here, a characteristic of the fifth embodiment is that the above-mentioned construction is realized by ion implantation for forming the N type layer from oblique upper side of the first gate insulation film 4 by using the first gate insulation film 4 as a mask after forming the gate electrode 4 as shown in Fig. 12.

That is, a middle concentration N type layer 11C is formed near the N+ type drain region 10 included in said N- type drain region 5B having the predetermined space (L) from the other

end portion of said gate ~~electrode 7~~ insulation 4 by ion-implanting phosphorus ion ($^{31}P^{+}$), for example, with about 160 KeV in acceleration voltage and about 2 x $10^{12}/cm^2$ in implantation ~~volume~~ dose from oblique upper side of the first gate insulation film 4 by using the first gate insulation film 4 on the gate insulation film 3 as a mask after the process of Fig. 4 described in the first embodiment. At this time, depending on thickness of the first gate insulation film 4, a space (L) from the end portion of the gate ~~electrode 7~~ insulation 4 to the position where the N type layer 11C is formed is adjusted freely by adjusting ion adjusting angle from oblique upper side of the first gate insulation film 4 (ion implantation of 30 degrees of oblique angle from vertical direction in the embodiment) freely.

Thus, in the fifth embodiment, the N type layer 7D having the predetermined space (L) from the gate ~~electrode 7~~ insulation 4 can be formed by ion implantation from oblique upper side of the first gate insulation film 4, and number of manufacturing processes can be decreased comparing with manufacturing method using the photo-resists PR2 and the side wall insulation film 13. Moreover, a space (L) from the end portion of the gate ~~electrode 7~~ insulation 4 to the position where the N type layer 11C is formed can be adjusted only by adjusting freely ion implantation angle at ion implantation, so that operation efficiency is good.

In the process using such the oblique ion implantation method, ion implantation may be carried out from oblique

direction using a photo-resist 12 as the above-mentioned second embodiment though the description shown in a figure is omitted. Further, ion implantation may be carried out from oblique direction using said side wall insulation film 13 as the third embodiment instead of the photo-resist 12.

According to the invention, since the lower concentration reverse conductive type drain region differ in high impurity concentration between the under part of the gate electrode through the first gate insulation film and the active region is formed, electric field concentration to the end portion of the gate electrode through the first gate insulation film is controlled so as to improve operation sustaining voltage.

The semiconductor device has high impurity concentration peak at the position of the predetermined depth in the substrate at region where is separated from the other end of the gate electrode and spans to a high concentration reverse conductive type drain region included in a low concentration reverse conductive type drain region, and forms a middle concentration reverse conductive type layer becoming low in high impurity concentration at region near surface of the substrate. Therefore, operation sustaining voltage further improves.

Especially, by forming said middle concentration reverse conductive type layer at the position separated the predetermined space from the end portion of the gate electrode through said first gate insulation film, higher sustaining

voltage becomes possible.